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| UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small> | Attorney Docket No. | 209665US2 |
| | First Inventor or Application Identifier | Seiichi M |
| | Title | SEMICONDUCTOR MEMORY INTEGRATED CIRCUIT AND ITS MANUFACTURING METHOD |
| jc860 U.S. PTO  | Assignee Name: | KABUSHIKI KAISHA TOSHIBA |
| | Assignee Address: | 72, Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken, JAPAN |

06/08/01

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g. PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification Total Sheets **36**
3. ☒ Drawing(s) (35 U.S.C. 113) Total Sheets **41**
Formals
4. ☐ Oath or Declaration Total Pages
 - a. ☐ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 C.F.R. §1.63(d))
(for continuation / divisional w/ box 17 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in
the prior application, see 37 C.F.R. §1.63(d)(2) and
1.33(b).
 - c. ☐ CD-ROM or CD-R in duplicate, large table or Computer
Program (Appendix)
 - d. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. ☐ Computer Readable Form (CRF)
 - b. Specification or Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ Paper
 - c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☒ Application Data Sheet. See 37 CFR 1.76
9. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ White Advance Serial No. Postcard
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Applicant claims small entity status.
See 37 CFR 1.27
16. ☒ Other: Notice of Priority, List of Inventor's Name
and Address, IDS/Related/List of Related
Cases, Cited Pending Applications (1)

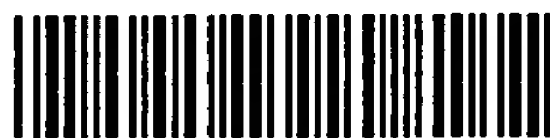
17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below:

- ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:
Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

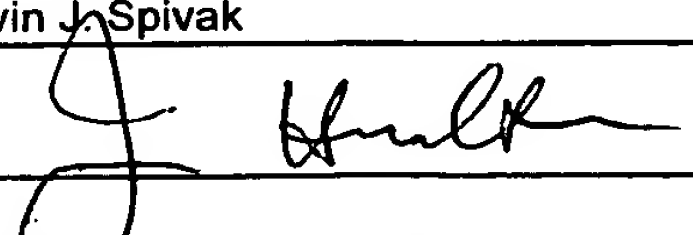
18. Amend the specification by inserting before the first line the sentence:

- ☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)
of application Serial No. Filed on
☐ Which was published in English
☐ Which was not published in English
☐ This application claims priority of provisional application Serial No. Filed

19. CORRESPONDENCE ADDRESS**22850**

(703) 413-3000

FACSIMILE: (703) 413-2220

| | | | |
|------------|---|-------------------|--------|
| Name: | Marvin J. Spivak | Registration No.: | 24,913 |
| Signature: |  | Date: | 6-8-01 |
| Name: | James D. Hamilton | Registration No.: | |

Registration No. 28,421

Docket No. 209665US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Seiichi MORI

SERIAL NO: New Application

FILING DATE: Herewith

FOR: SEMICONDUCTOR MEMORY INTEGRATED CIRCUIT AND ITS MANUFACTURING METHOD

FEE TRANSMITTAL

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

| FOR | NUMBER FILED | NUMBER EXTRA | RATE | CALCULATIONS |
|--|-----------------|-----------------|-----------|--------------|
| TOTAL CLAIMS | 20 - 20 = | 3 | × \$18 = | \$0.00 |
| INDEPENDENT CLAIMS | 6 - 3 = | 3 | × \$80 = | \$240.00 |
| <input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS (If applicable) | | | + \$270 = | \$0.00 |
| <input checked="" type="checkbox"/> LATE FILING OF DECLARATION | | | + \$130 = | \$130.00 |
| BASIC FEE | | | | \$710.00 |
| TOTAL OF ABOVE CALCULATIONS | | | | \$1,080.00 |
| <input type="checkbox"/> REDUCTION BY 50% FOR FILING BY SMALL ENTITY | | | | \$0.00 |
| <input type="checkbox"/> FILING IN NON-ENGLISH LANGUAGE | | | + \$130 = | \$0.00 |
| <input type="checkbox"/> RECORDATION OF ASSIGNMENT | | | + \$40 = | \$0.00 |
| TOTAL | | | | \$1,080.00 |

Please charge Deposit Account No. 15-0030 in the amount of

A duplicate copy of this sheet is enclosed.

A check in the amount of \$1,080.00 to cover the filing fee is enclosed.

The Commissioner is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to Deposit Account No. 15-0030.

A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Marvin J. Spivak

Registration No. 24,913

James D. Hamilton
Registration No. 28,421

Date: 6-8-01



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Docket No. 209665US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Seiichi MORI

FILING DATE: Herewith

FOR: SEMICONDUCTOR MEMORY INTEGRATED CIRCUIT AND ITS MANUFACTURING METHOD

LIST OF INVENTOR'S NAME AND ADDRESS

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Listed below are the name and address of the inventor for the above-identified patent application.

Seiichi MORI

Ota-ku, JAPAN

A declaration containing all the necessary information will be submitted at a later date.

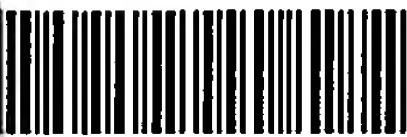
Respectfully Submitted,

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09876543210



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OSMMN 11/98)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Seiichi MORI

GAU:

SERIAL NO: NEW APPLICATION

EXAMINER:

FILED: HEREWITH

FOR: SEMICONDUCTOR MEMORY INTEGRATED CIRCUIT AND ITS MANUFACTURING METHOD

REQUEST FOR PRIORITY

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

- ☐ Full benefit of the filing date of U.S. Application Serial Number, filed, is claimed pursuant to the provisions of 35 U.S.C. §120.
- ☐ Full benefit of the filing date of U.S. Provisional Application Serial Number, filed, is claimed pursuant to the provisions of 35 U.S.C. §119(e).
- ☒ Applicants claim any right to priority from any earlier filed applications to which they may be entitled pursuant to the provisions of 35 U.S.C. §119, as noted below.

In the matter of the above-identified application for patent, notice is hereby given that the applicants claim as priority:

| <u>COUNTRY</u> | <u>APPLICATION NUMBER</u> | <u>MONTH/DAY/YEAR</u> |
|----------------|---------------------------|-----------------------|
| JAPAN | 2000-174127 | June 09, 2000 |
| JAPAN | 2001-171612 | June 06, 2001 |

Certified copies of the corresponding Convention Application(s)

- ☐ are submitted herewith
- ☒ will be submitted prior to payment of the Final Fee
- ☐ were filed in prior application Serial No. filed
- ☐ were submitted to the International Bureau in PCT Application Number .
Receipt of the certified copies by the International Bureau in a timely manner under PCT Rule 17.1(a) has been acknowledged as evidenced by the attached PCT/IB/304.
- ☐ (A) Application Serial No.(s) were filed in prior application Serial No. filed ; and
(B) Application Serial No.(s)
- ☐ are submitted herewith
- ☐ will be submitted prior to payment of the Final Fee

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.


Marvin J. Spivak
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James D. Hamilton
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JC971 U.S. PTO
09/876019
06/08/01